REMARKS/DISCUSSION OF ISSUES

Claims 8 and 13-17 are pending in the application. Applicants have amended claim 17 for clarification.

Applicants respectfully request that the Examiner **acknowledge the claim for priority** and receipt of certified copies of the priority document which was submitted in the parent application.

The Examiner is also respectfully requested to **state whether the drawings are acceptable**.

Reexamination and reconsideration are respectfully requested in view of the following remarks.

35 U.S.C. § 112

The Office Action rejected claims 14-17 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite

Applicants respectfully traverse that rejection for at least the following reasons.

Claim 14

The Office Action has stated that the term "a differential pair of transistors" is unclear, and asks whether they are shown in any of the drawings.

At the outset, Applicants respectfully submit that there is no requirement under 35 U.S.C. § 112, second paragraph to show anything in the drawings. Nevertheless, for example: FIG. 2 shows two different set of differential pairs of transistors (204 and 206); and FIGs. 3 and 4 show a differential pair of transistors 304. Meanwhile, the specification specially states at page 8, lines 5-6 that:

> "*The voltage-measuring device is in Figure 2 shown as a differential pair of transistors.*"

Furthermore, Applicants respectfully submit that anyone of ordinary skill in the art would understood what is meant by the well-known phrase "differential pair of

transistors," particularly in light of the specification and FIGs. 2-4, as discussed above. Indeed, the term is very well known in the art, as shown for example in the attached list of definition's from the Internet site of a leading integrated circuit manufacturer (Intersil).

Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claim 14 under 35 U.S.C. § 112, second paragraph.

Claim 15

The Office Action has stated that the term "a differential pair of transistors" is unclear, and asks whether they are shown in any of the drawings. Applicants have already addressed this issue with respect to claim 14 above.

The Office Action has also stated that the term "means for toggling connections" is unclear, and asks whether it is shown in any of the drawings.

At the outset, Applicants respectfully submit that there is no requirement under 35 U.S.C. § 112, second paragraph to show anything in the drawings. Nevertheless, for example, FIG. 2 shows means for toggling connections as toggle switch 216. Meanwhile, the specification describes operation of an exemplary embodiment of a means for toggling connections 216, for example, at page 8, lines 16-20.

Furthermore, Applicants respectfully submit that anyone of ordinary skill in the art would understood what is meant by the phrase "means for toggling connections," particularly in light of the specification as cited above.

Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claim 15 under 35 U.S.C. § 112, second paragraph.

Claim 16

The Office Action has stated that the term "means for successively connecting the voltage measuring device" is unclear, and asks where it is shown in any of the drawings.

At the outset, Applicants respectfully submit that there is no requirement under 35 U.S.C. § 112, second paragraph to show anything in the drawings. Nevertheless, for example, FIG. 3 shows means for successively connecting the

voltage measuring device 304 to the segment of the signal line and to a segment of a second signal line, as switches 306 and 308. Meanwhile, the specification describes operation of an exemplary embodiment of means for successively connecting the voltage measuring device to the segment of the signal line and to a segment of a second signal line (306, 308), for example, at page 8, line 33 - page 9, line 10.

Furthermore, Applicants respectfully submit that anyone of ordinary skill in the art would understood what is meant by the phrase "means for successively connecting the voltage measuring device," particularly in light of the specification as cited above.

Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claim 16 under 35 U.S.C. § 112, second paragraph.

Claim 17

The Office Action has stated that it is unclear whether "first and second sub-circuits" have been claimed.

By this Amendment, Applicants have amended claim 17 to more clearly indicate that the first and second sub-circuits have been claimed. For example, an exemplary signal line 714 extending between first and second sub-circuits 704 and 706 is shown in FIG. 7 and discussed at page 11, lines 20-22.

Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claim 17 under 35 U.S.C. § 112, second paragraph.

OBVIOUSNESS-TYPE DOUBLE PATENTING REJECTION

Applicants acknowledge the obviousness-type double patenting rejection of claims 8 and 13 over U.S. Patent 6,239,604. The Examiner has not accepted the Terminal Disclaimer filed on 31 January 2003. Applicants have filed subsequent Terminal Disclaimers on 15 July 2003 and 29 October 2003 (copies attached hereto). In the event that neither of these Terminal Disclaimers are deemed acceptable, then once this application is deemed by the Examiner otherwise to be in condition for allowance such that no further amendments are needed, Applicants will be prepared to sign and submit another proper Terminal Disclaimer.

35 U.S.C. § 102

The Office Action rejected claims 8 and 13 under 35 U.S.C. § 102 over Pellegrini U.S. patent 5,483,173 ("Pellegrini").

Applicants respectfully traverse those rejections for at least the following reasons.

Claim 8

Among other things, the inspection method of claim 8 includes: (1) measuring a voltage over a segment of a signal line; and (2) determining a signal current flowing through the signal line on the basis of the voltage and the resistance of the segment of the signal line.

Applicants respectfully submit that Pellegrini does not disclose any inspection method including such features.

At the outset, as taught by Pellegrini the op amp 5 and voltage source 7, mentioned in the Office Action, are actually part of a current limiting circuit 4 of the power stage (see col. 1, lines 45-50; col. 2, lines 1-5). These circuit elements do not perform any inspection of the integrated circuit on the basis of any measured voltage and inherent resistance, as featured in claim 8.

Pellegrini teaches that it is important to measure the current value that triggers the operation of the current limiting circuit 4 (col. 1, lines 17-23). Indeed, the whole point of Pellegrini's disclosure is to provide an improved structure for measuring the current value that triggers operation of the current limiting circuit 4 ("the intervention condition") during a wafer test stage.

Pellegrini discloses two separate inspection or test stages where this particular current value is to be measured: (1) the wafer test stage; and (2) the final test stage (see, e.g., col. 1, lines 11-16).

In the first case, Pellegrini teaches that:

> "Metal strip 18 terminates at a second pad 18 smaller than pad 17 and defining input **terminal 13 to which a probe is applied for measuring current I_{L1}** through transistor 2 at the wafer test stage."

In the second case, Pellegrini teaches that:

> "Strip 15 is connected . . . at the other end to a pad 17 defining input terminal 12 and to which is applied **a probe (not shown) for measuring current I_{L2}** through the transistor 2 at the final test stage"

col. 3, lines 32-36 (emphasis added).

So, in neither case does Pellegrini teach measuring a voltage over a segment of a signal line; and determining a signal current flowing through the signal line on the basis of the measured voltage and the resistance of the segment of the signal line. Instead, for both tests, Pellegrini teaches that a probe at an input terminal (12 or 13) measures the current.

Thus, Pellegrini merely discloses a method by which the wafer test can be performed at a scaled-down current value for the intervention condition (i.e., that triggers the current limiting circuit 4) compared to the real, operating current value for the intervention condition. That is, a known scaling factor, i.e. $(R_s + R_{s1})/R_s$, can be used to determine the real, operating current value for the intervention condition (I_{L2}) from the measured, scaled-down current value for the intervention condition (I_{L1}). See Pellegrini at col. 4, line 15.

Therefore, Pellegrini does not disclose any inspection method including measuring a voltage over a segment of a signal line, and determining a signal current flowing through the signal line on the basis of the voltage and the resistance of the segment of the signal line.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 8 is patentable over Pellegrini.

Claim 13

Among other things, in the integrated circuit of claim 13, a voltage measuring device is adapted to measure a voltage over a segment of a signal line, and a current measuring device determines a current on the basis of the measured voltage and an inherent resistance of the segment.

Applicants respectfully submit that Pellegrini does not disclose any integrated circuit including such features.

As explained above, elements 5, 7, 20 and 21, cited in the Office Action, do not comprise a current measurement device, but rather comprise a current limiting circuit 4 of the power stage (MOS transistor 2) (see, e.g., col. 1, lines 46-50). They do not measure a voltage over a segment of a signal line, or determine a current on the basis of the measured voltage and an inherent resistance of the segment.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 13 is patentable over Pellegrini.

CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 8 and 13-17 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (703) 715-0870 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment (except for the issue fee) to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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Date: 8 January 2004

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